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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,567	12/28/2000	Brian Tse Deng	TI-29958	9822

23494 7590 10/19/2004

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,567	DENG ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-13,15-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13,15-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,8,15,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maemura (patent No. 5,455,936) in view of Miyake (patent No. 6,681,280) or Yoshioka (patent No. 6, 038,661).

3. Maemura taught the invention as claimed including a data processing ("DP") system comprising:

a) Program memory (102)(e.g., see fig.3 and col. 5 lines 40-58);

b) Instruction execution circuitry (101) coupled to program memory (e.g., see fig. 3);

c) Breakpoint address register (104) (e.g., see fig. 3);

d) Address compare circuitry (106) (e.g., see fig. 3) for comparing a value on the address bus to a value in the breakpoint address register, the compare circuitry providing a breakpoint signal upon detection of a valid breakpoint address comparison (e.g., see col. 4, line 53-col. 5 line10, and col. 5, lines 30-58);

e) Multiplexer (502,103) interposed between the program memory and program execution circuitry (e.g., see figs 7, and 3) for inserting a debug instruction in the execution circuitry upon receipt of the breakpoint signal, wherein the debug instruction

is substituted for an instruction in a program memory address pointed to by the program counter (e.g., see col. 6, lines 58-67).

4. Maemura did not expressly detail (claim 1) a program counter. However, The use of a register to store the address of the instruction currently being addressed or executed during execution of a program was well known in the DP art to be called the program counter. Since Maemura taught a system that addressed instructions via an instruction bus and tested whether the address on the bus was a particular address for replacing the instruction to be executed it would have been obvious to one of ordinary skill that the address on the bus comprised the address of the current instruction. Consequently to maintain the address on the address bus one of ordinary skill would have been motivated to maintain the address of the current instruction that was on the bus in a register namely a program counter.

5. Maemura did not expressly detail (claims 1,8,15) storing of the program counter address in a register as a return address from a debug monitor routing so after the debug was finished the system could return to the program at the proper location. Miyake taught this limitation (e.g., see col. 15, lines 7-27,col. 15, line 66-col.16, line 23, and col. 17, lines 1-30). Also Yoshioka taught this limitation (e.g., see col. 9, lines 21-41, col. 10, lines 30-47, and col. 12, line 20-64).

6. The feature of pushing of the address stored in the program counter copy register onto a stack (claim 20), was not specifically detailed by Maemura. With respect to the rejection using the Miyake reference the feature of storing program counter

on the stack, however, was well known in the art at the time of the claimed invention. With respect to the rejection using Yoshioka on the other hand, Yoshioka taught that the prior art taught this feature of storing values of the program counter onto stack region (e.g., see col. 1, lines 30-52). Also in the Yoshioka system at least one value of the program counter comprised the value stored in the program copy counter register (e.g., see col. 9, lines 21-41, col. 10, lines 30-47, and col. 12, line 20-64).

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Maemura and Miyake or Yoshioka. Both Miyake and Yoshioka taught storing the program counter value for a breakpoint stored in a separate register as discussed above. One of ordinary skill would have been motivated to incorporate this feature of separate register for program counter for a breakpoint used in a debug routine at least to provide more efficient access to the program counter when return from a debug routine was needed.

8. Claims 2,3,5,10,11,13,16,17,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maemura in view of Miyake (patent No. 6,681,208) or Yoshioka (patent No. 6, 038,661) as applied to claims 1,8,15 above, and further in view of Yishay et al. (patent No. 5,717,851).

9. Yishay taught (claims 2,3,10,11,16,17) reading a breakpoint address from the stack (i.e., stack break point location) or register (i.e., breakpoint register) or state of program counter (e.g., see col. 15, lines 31-40 and col. 16, lines 36-68) and compare circuitry (42) to compare the value of the stack address with the breakpoint register for

providing a stack trap signal (e.g., see figs.2, 7, and col. 16, lines 38-52). Yishay did not specify a stack pointer register. The current location being accessed would have been required to have been available to the system in order to access the stack. Further, the use of a register to store the current address of the stack namely a stack pointer register (so that the address was available to the system and not lost) was well known in the art at the time of the invention.

10. As to the use of mutiplexer for inserting the instruction Maemura taught a multiplexer(502,103) for inserting the debug instruction (e.g., see col. 6, lines 58-67).

11. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Maemura and Yishay. The addition of the use of stacks to store the breakpoint data as taught by Yishay would have provided means to quickly access the breakpoint data for comparison. Therefore one of ordinary skill would have been motivated to incorporate the teachings of Yishay at least for the use of a stack to store the breakpoint address for comparison to provide quick access to the breakpoint address.

12. As per claims 5,13, Maemura taught a jump to a monitor program that operated in the background (e.g., see col. 3, lines 46-col. 4, line 12 and col. 5, lines 31-64).

13. As per claim 18, Yishay taught sending status signals to external to the system integration element (i.e., at least to the CPU) (e.g., see fig. 1 and col. 11, lines 34-61)

14. Claims 4,9,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maemura in view of Miyake (patent No. 6,681,208) or Yoshioka (patent No. 6, 038,661) as applied to claims 1,8,15 above, and further in view of Favor (patent No. 6,336,178).

15. Favor taught single-step traps in a system that performed breakpoint traps (e.g., see col. 59, lines 54-63).

16. One of ordinary skill in the DP art would have been motivated to use single step traps of Favor to at least to debug each instruction in Maemura's system separately, and more precisely determine the effect processing instructions.

17. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maemura in view of Miyake (patent No. 6,681,208) or Yoshioka (patent No. 6, 038,661) as applied to claims 1,8,15 above, and further in view of Jaggar (patent No. 6,343,358).

18. Jaggar taught the debug coprocessor included a bank of watchpoint registers and a bank of breakpoint registers and control registers that store flags that enable or disable the associated breakpoint of watch point registers (e.g., see col. 3, line 47-col. 4, line 19).

19. One of ordinary skill would have been motivated to incorporate the teachings of Jaggar and Maemura because the Jaggar teaching of use of banks of breakpoint and watchpoint registers would have allowed the debug system to scan large number of instructions (e.g., see col. 1, lines 7-19).

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER